

TGB2000S-IP, GPS Baseband IP Solution

Overview

- Navigation S/W can be ported into a customer host processor.
- Tailored for customer interface and applications
- High accuracy with adaptive processing against a variety of signal level and variation
- Integrated signal processing with navigation S/W against multipath environments
- Resource sharing techniques and configurable architecture
- Low power structure and managements
- Matured proprietary CDM technology

Features

High Performance GPS Navigation

- Adaptive operation for high sensitivity and dynamics
- Advanced tracking loop and filter techniques against multipath environments
- Patented fast acquisition architecture
- SBAS support
- Real-time raw data and timing control processing

Multiple Environments Support

- Stationary, land vehicle, high dynamic airborne and military area

Multiple Protocol Support

- NMEA protocol
- TGB protocol
- Satellites and PVT information
- Customer configuration and masks
- Test and monitoring

A-GPS Support

- Fast position fix with aiding information

Architecture Highlights

- GPS core H/W and host navigation S/W partitioning
- Flexible IP structure
- Customizable GPS core structure for size optimized application
- Customizable host and peripherals interface support (AHB/EMI, various peripherals)
- Various IP type (netlist, GDS support)
- BBR and RTC for hot start and navigation parameter storage
- Expansive peripherals with UARTs, I2Cs, SPIs, Timers, Watchdog Timer, 1PPS, Interrupt controller, and GPIOs

Applied Products

- RTLS-GPS chip (2009)
- WiFi-GPS connectivity chip (2010)

Specifications

Position Accuracy

- Autonomous CEP¹ < 2m
- SBAS < 1.5m

TTFF²

- Hot < 1s
- Cold < 30s
- Aiding < 1s

Sensitivity

- Acquisition -145dBm
- Navigation -158dBm
- Tracking -162dBm

Receiver

- Tracking signal
- Max update rate
- Protocol support

L1 C/A, SBAS
2 Hz
NMEA
TGB binary

Host I/F

- AHB
- EMI

IP Type

- S/W : Host Navigation S/W Lib.
- H/W : netlist, GDS

Expansive peripherals

- UARTs
- I2Cs
- SPIs
- Timers
- 1PPS
- Interrupt Controller
- GPIOs

- 1. Static, -130dBm
- 2. 50%, -130dBm

Interface

- GPS RF front-end chip interface
- Host CPU interface : AHB/EMI interface (can be customized)
- RF clock : TCXO (16,368, 16.367667 or 16.369 MHz)
- RTC clock : XTAL (32.768KHz)

Host Requirements

- MIPS : ≥ 20 (Avg.)
- Memory : ≥ 256KB (program memory + data memory)
- Host I/F : EMI, AHB (or customized I/F)

